



# Method to mitigate an insertion/deletion error in bit-patterned media recording systems

Santi Koonkarnkhai<sup>1,\*</sup> and Piya Kovintavewat<sup>1</sup>

<sup>1</sup>Data Storage Technology Research Center, Nakhon Pathom Rajabhat University,  
Nakhon Pathom 73000, Thailand

## Abstract

Bit-patterned media recording (BPMR) is a feasible technology to increase an areal density of hard disk drives. In practice, the insertion and deletion (Ins/Del) error is one of major problems in BPMR systems. This Ins/Del error arises from a write synchronization error, which may lead to an error burst at data detection process. In this paper, we propose a method to mitigate an Ins/Del error for BPMR systems, which uses a trellis-based detection technique together with the Varshamov and Tenengolts (VT) code to correct the Ins/Del error. We compare the performance of different methods in BPMR systems. Simulation results indicate that the proposed method can enhance the system performance in the presence of Ins/Del error. In addition, the proposed method is also robust to the change in the probability of Ins/Del occurrence.

**Keywords:** bit-patterned media recording, insertion/deletion error, write synchronization error

**Article history:** Received 12 January 2017, Accepted 4 August 2017

## 1. Introduction

Currently, the perpendicular magnetic recording (PMR) technology is employed in hard disk drives. However, this PMR technology is approaching its capacity limit up to 1 Tbit/in<sup>2</sup>, known as a superparamagnetic limit [1]. Bit-patterned media recording (BPMR) is a promising technology to avoid the thermal instability of magnetic material, which can help increase an areal density (AD) up to 4 Tbit/in<sup>2</sup>. Moreover, when BPMR combines with an energy assisted technology, e.g., a heated-dot magnetic recording (HDMR) technology [2], the AD can be further increased up to 10 Tbit/in<sup>2</sup> [1].

In BPMR, each data bit is recorded on an isolated single grain magnetic called as “island”, which is separated by non-magnetic material. To achieve high storage capacity, the spacing between the islands both in the along- and across-track directions must be reduced. This will cause the two-dimensional (2-D) interference in the BPMR system, consisting of inter-symbol interference (ISI) and inter-track interference (ITI), which can deteriorate the system performance, especially at high ADs [2]. Furthermore, the BPMR system also encounters an insertion and deletion (Ins/Del) error, which can cause an error burst at data recovery process [3].

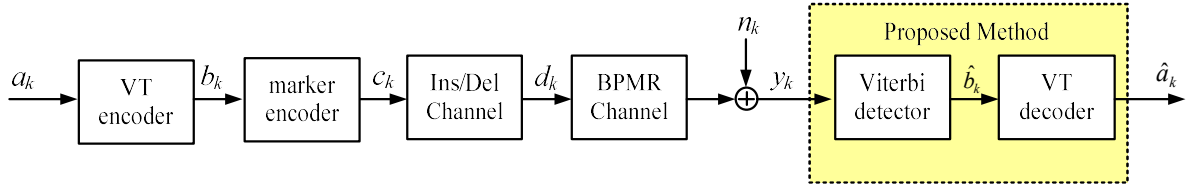
Generally, the Ins/Del error may result from mis-synchronization between the write clock and the island positions [4], which will be known as a write synchronization error. Moreover, the dead islands, the fluctuation of magnetic saturation, and the located random phase drift can also cause the Ins/Del error. Although the probability of Ins/Del errors occurred in BPMR are very small [5], this Ins/Del error can easily

cause a burst error in data detection process, which could exceed the correction capability of conventional error-correction codes (e.g. Reed-Solomon code, low-density parity-check code, etc.). Thus, the problem of Ins/Del errors is a challenging problem in BPMR systems. Essentially, a special code to combat the Ins/Del error is needed.

Many works have been proposed to deal with the Ins/Del error [6 - 8]. For example, Seller [6] presented a simple method to detect and correct the Ins/Del error by using a so-called “marker code”, which is used in several digital communication systems [9], including a magnetic recording system [10]. Nonetheless, this marker code cannot find the exact location of the inserted or deleted bit. Then, Kuznetsov and Erden [7] proposed to utilize the Varshamov and Tenengolts (VT) code to detect and correct the Ins/Del error; however, this method is sensitive to an additive noise. Koonkarnkhai *et al.* [8] introduced a method to detect the Ins/Del error in BPMR systems based on the trellis structure, which is performed inside the Viterbi detector; however, they did not mention a method to correct this Ins/Del error. Therefore, this paper proposes a method to mitigate the Ins/Del error in a BPMR system, which employs the trellis-based detection in conjunction with the VT code. Specifically, we utilize a technique in [8] to detect the Ins/Del error and then use the VT code to correct it.

The rest of this paper is organized as follows. After describing a partial response channel model with Ins/Del error in Section 2, the marker code is described in Section 3. Section 4 presents the proposed method,

\*Corresponding author; e-mail: santi@webmail.npru.ac.th



**Figure 1** BPMR channel model with the proposed method to suppress the Ins/Del error

and simulation results are given in Section 5. Finally, Section 6 concludes this paper.

## 2. Channel model

A BPMR channel model with the proposed method is shown in Figure 1. We consider a single read head, and a binary input sequence  $a_k \in \{-1, 1\}$  with bit period  $T$  is encoded by a VT code followed by a marker code. Next, a sequence  $c_k$  is fed to the Ins/Del channel [10] to include the effect of Ins/Del error in a system so as to obtain a sequence  $d_k$ . Additionally, we assume the worst case scenario that each data sector contains one Ins/Del error. The sequence  $d_k$  is sent to BPMR channel. This paper uses a partial response class-2 (PR2) to represent a BPMR channel response (main track only and not including the ITI effect), which can be written as  $H(D) = 1 + 2D + D^2$  where  $D$  is a unit delay operator. Then, the readback signal  $y_k$  can be given by

$$y_k = \sum_i h_i d_{k-i} + n_k \quad (1)$$

where  $h_k$ 's are the coefficients of a PR2 channel [8], and  $n_k$  is an additive white Gaussian noise (AWGN) with zero mean and variance is  $\sigma^2$ .

At a conventional receiver, the readback signal  $y_k$  is fed to the conventional Viterbi detector [11] to determine the most likely data sequence,  $\hat{b}_k$ . Then, the data sequence  $\hat{b}_k$  is sent to the marker decoder to detect and correct the Ins/Del error so as to obtain an estimated input sequence  $a_k$ . On the other hand, for the proposed method, the detection of Ins/Del errors will be performed inside the Viterbi detector as presented in [8], which will output the Ins/Del error location and a data sequence  $\hat{b}_k$  for the VT decoder for Ins/Del correction.

## 3. Existing method

A marker code is employed in many communication systems [6, 9], e.g., a magnetic recording system [10]. The marker code was proposed by Seller [6], which is a simple code for encoding and decoding. To encode a data sequence, a marker pattern of  $r$  bits is inserted every  $p$  bits, where  $r > 1$  and  $p > 1$  are an integer number. Then, its code word can be written as

$$x_1, \dots, x_p, m_1, \dots, m_r, x_{p+1}, \dots, x_{2p}, \dots, \quad (2)$$

where  $x_k$  is a data input sequence and  $m_k$  is a marker pattern. To decode a data sequence, the detected sequence is fed to a marker decoder by using the 2 consecutive marker patterns to determine the Ins/Del error, based on a table lookup as given in Table 1 [6], where  $X$  is either  $-1$  or  $+1$  and  $K$  is  $\{p, 2p, \dots\}$  in (2). Note that we will use the marker pattern  $\mathbf{M} = [1 \ -1 \ -1]$  with  $r = 3$  bits to compare with the proposed method in this paper.

## 4. Proposed method

This paper proposes a method to detect and correct an Ins/Del error in a BPMR system. To do so, an input data sequence will be encoded by a VT code followed by a marker code. Then, for Ins/Del error detection, we use a marker code with pattern  $\mathbf{M} = [1 \ -1 \ -1 \ -1 \ 1]$  inserted every  $m$  bits, and detect an Ins/Del error inside the Viterbi detector as explained in [8] for a PR2 channel. Figure 2 describes how to detect the Ins/Del error in the Viterbi detector, which can be explained as follows. Let  $\hat{\mathbf{b}}_{n+1}^{n+l} = [\hat{b}_{n+1}, \hat{b}_{n+2}, \dots, \hat{b}_{n+l}]$  denote a set of decoded bits from time  $n+1$  to  $n+l$  obtained from the Viterbi detector and  $l = 5$  is the length of  $\mathbf{M}$ .

If  $\hat{\mathbf{b}}_{n+1}^{n+l} = \mathbf{M}$ , it means no insertion or deletion error in a system. However, the insertion error is detected if  $\hat{\mathbf{b}}_{n+2}^{n+l+1} = \mathbf{M}$ , whereas the deletion error is detected if  $\hat{\mathbf{b}}_n^{n+l-1} = \mathbf{M}$ . Furthermore, if all conditions are not satisfied, we cannot conclude if the system encounters an Ins/Del error or not. In this case, we need to look at the path metric difference evaluated in the Viterbi detector. Specifically, the path metric difference will be calculated at the end of the marker code, which can be computed from

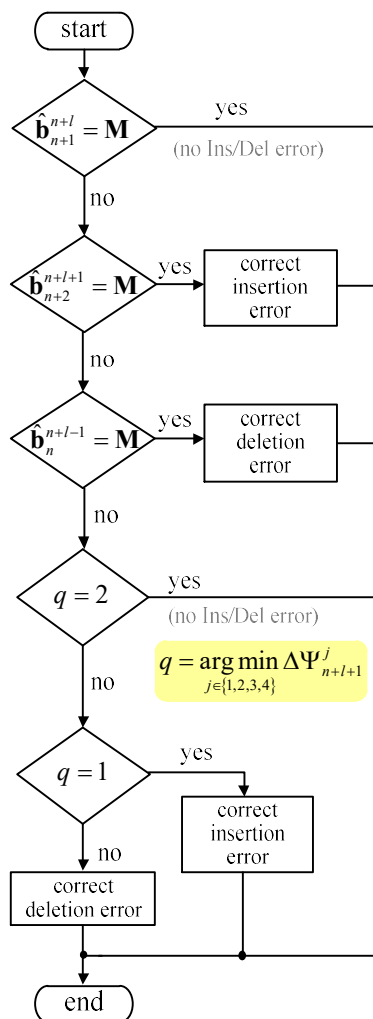
$$\Delta\Psi_{n+l+1}^j = \left| \Psi_{n+l+1}^j - \Psi_{n+l+1}^{i_{n+1}} \right|, \quad (3)$$

where  $i_{n+1}$  is the starting state at time  $n+1$  associated with the survival path arriving in state  $j$  at time  $n+l+1$ , and  $j \in \{1, 2, 3, 4\}$ . Let  $q$  denote the state that yields a minimum  $\Delta\Psi_{n+l+1}^j$ , that is

$$q = \arg \min_{j \in \{1, 2, 3, 4\}} \left\{ \Delta\Psi_{n+l+1}^j \right\} \quad (4)$$

**Table 1** Table lookup for marker code [6]

Maker pattern after $x_K$	Maker pattern after $x_{K+1}$	Analysis	Correction
1 -1 -1	1 -1 -1	No insertion or deletion error	-
X 1 -1	X 1 -1	An insertion error	Take out received bit $x_{K-p/2+1}$ for $p$ even $x_{K-p/2+1/2}$ for $p$ odd
-1 -1 -1 -1 -1 1 1 -1 1 1 1 1 1 -1 -1	X 1 -1	Error in marker pattern and an insertion error	Take out a bit in marker pattern
-1 -1 X	-1 -1 X	A deletion error	Add a bit between $x_{K-p/2}$ and $x_{K-p/2+1}$ for $p$ even $x_{K-p/2-1/2}$ and $x_{K-p/2+1/2}$ for $p$ odd
1 1 -1 -1 1 -1 -1 -1 1 1 -1 -1 1 1 1	-1 -1 X	Error in marker pattern and a deletion error	Add a bit in marker pattern



**Figure 2** Flow chart to explain how the proposed detection method performs [8]

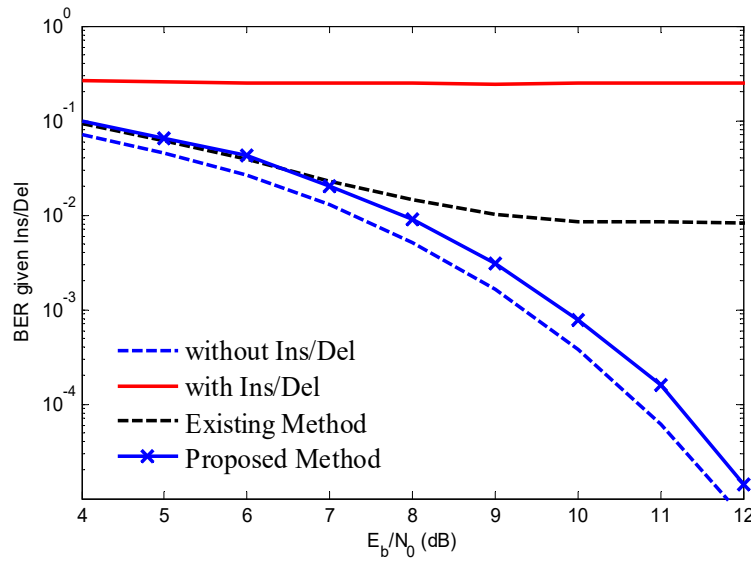


Figure 3 BER performance of different schemes

Table 2 Complexity comparisons of different methods per codeword

Method	Multiplication operator	Addition/Comparison operator
Existing method	-	$2r$
Proposed method	$10Q + 248$	$10Q + 2r + 506$

For a PR2 channel with the marker code of pattern  $\mathbf{M}$ , it is easy to use the state  $q$  to determine the Ins/Del error. Specifically, it has no Ins/Del error if  $q = 2$ ; an insertion error is presented if  $q = 1$ ; and a deletion error is occurred if  $q \in \{3,4\}$ . To correct the Ins/Del error, we employ the VT code. The trellis-based Ins/Del detection will output the location of the Ins/Del error to the VT decoder [12], which can effectively correct one Ins/Del error per codeword [7].

### 5. Experimental results

Consider the BPMR channel model with an Ins/Del error in Figure 1. The signal-to-noise ratio (SNR) is defined as

$$\frac{E_b}{N_0} = 10 \log_{10} \left( \frac{\sum_k |h_k|^2}{2R\sigma^2} \right) \quad (5)$$

in decibel (dB), where  $E_b$  is an energy per bit and  $R$  is the overall code rate of the system. One data sector at the input of the Ins/Del channel contains 4128 bits for all systems. The Ins/Del error will occur during the write process with a probability of 0.5, where the location of the error is a uniform distribution within a sector.

The bit-error rate (BER) is computed based on a minimum number of 10000 data sectors and 1000 error bits, and we call it “BER given Ins/Del.” Note that the existing method uses the marker pattern with  $r = 3$  bits, i.e.  $\mathbf{M} = [1 \ -1 \ -1]$ , inserted every  $p = 255$

data bits, where its overall code rate is 0.98. On the other hand, the proposed method employs a rate-247/255 (0.968) VT code and a rate-255/260 (0.98) marker code, where the overall code rate is  $R = 0.95$ .

Figure 3 shows the BER performance of different schemes, where the performance of the system without Ins/Del errors is denoted as “without Ins/del.” Clearly, without a technique to suppress Ins/Del errors, the system performance is unacceptable, referred to as “with Ins/Del.” It is apparent that the proposed method performs better than the existing one [6]. We also compare the BER performance of different schemes in terms of the probability of insertion error ( $P_i$ ) as illustrated in Figure 4. Evidently, the proposed method is robust to the change of  $P_i$ , especially at high  $P_i$ . Furthermore, the BER performance of different schemes in terms of the probability of deletion error ( $P_d$ ) looks similar to that of  $P_i$  (not shown here). Finally, Figure 5 depicts the BER performance of different schemes in terms of  $P_i$  and  $P_d$ , where the probability of Ins/Del errors is  $P_i + P_d$ , where  $P_i$  and  $P_d$  has equal probability. It is clear that the proposed method performs better than the existing one and is robust to the change of the probability of Ins/Del error at an expense of increased complexity as shown in Table 2, where  $Q$  is the number states in trellis. Here, the complexity is defined as the number of addition and multiplication operators used in each algorithm.

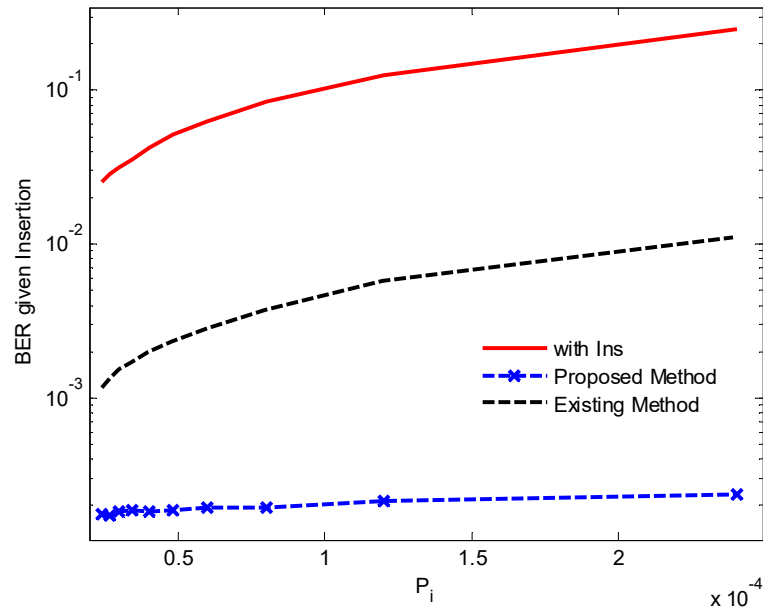


Figure 4 BER performance in terms of the probability of insertion error ( $P_i$ )

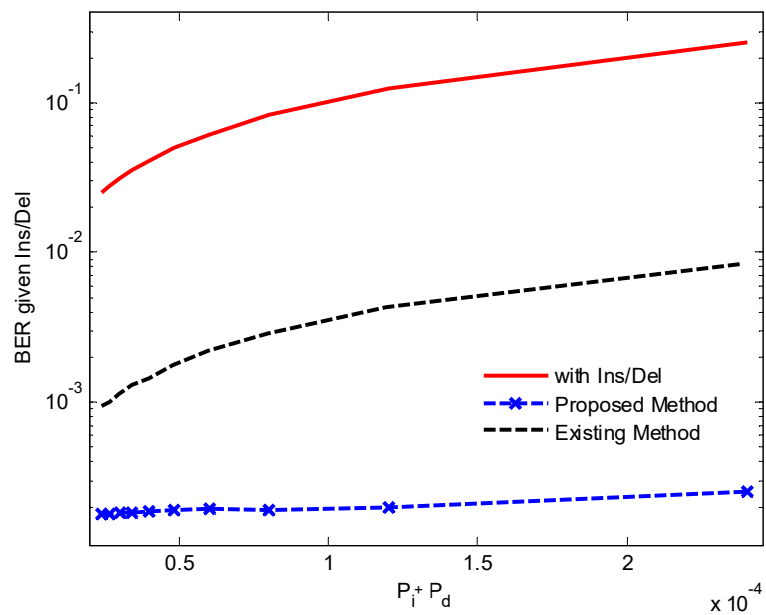


Figure 5 BER performance in terms of the probability of Ins/Del errors ( $P_i + P_d$ )

## 6. Conclusions

The Ins/Del error is a main problem in a BPMP system because it can yield an error burst at the data detection process, which could easily exceed the correction capability of conventional error-correction codes, such as RS and LDPC codes. Thus, the special code for an Ins/Del error is required to mitigate its effect. This paper proposes to utilize the trellis-based technique [8] to detect the Ins/Del error and employs the VT code to correct it. As shown in simulation, the proposed method is superior to the existing one in

terms of BER and is also robust to the change in the probabilities of insertion and deletion ( $P_i$  and  $P_d$ ). However, it should be noted that the proposed method has more complexity than the existing one. Consequently, there is a trade-off between performance improvement and increased complexity, when using the proposed method to combat the Ins/Del error. Finally, all advantages gained by the proposed method need to be balanced against the increased implementation cost caused by the VT code and trellis-based detection technique.

### Acknowledgements

This project was supported by a grant number GB-60\_10 from Research and Development Institute, Nakhon Pathom Rajabhat University. The authors would like to thank the anonymous reviewer for their helpful comments.

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